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Re: U.S. Patent No. 7,256,865
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For: **Methods and Apparatuses for Applying Wafer-Alignment Marks**
Patentees: CONSOLINI *et al.*
Our Ref: 1857.7040000

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Power of Attorney to Prosecute Applications Before the USPTO; and
2. Statement Under 37 C.F.R. 3.73(b).

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

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JDE/awt
Enclosures

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